IN THE CLAIMS

Please amend the claims as follows:

1. (Currently amended) ~~Arrangement including~~An apparatus being connected between a display device ~~(303)~~ and a processor ~~(301)~~ controlling the display device, ~~wherein the arrangement comprises~~comprising: ~~an intelligent display device connection interface (302) integrated in the display device,~~

a memory bus ~~(304)~~ connected to the processor, and

an adaptor circuit connected between the memory bus and a display device connection interface integrated in the display device,

wherein the apparatus is configured ~~(301) in order~~ to realize signaling between the processor ~~(301)~~ and the display device connection interface ~~(302)~~, and

wherein the ~~an~~ adapter circuit ~~(402) in order~~is configured to match signals between the memory bus ~~(401,510)~~ and the display device connection interface ~~(404,540)~~ by synchronizing the signals of the memory bus in an order required by the display device.

2. (Currently amended) The ~~arrangement~~ apparatus according to claim 1, wherein the ~~intelligent~~ display device connection interface is a medium speed screen interface ~~MeSSI (Medium Speed Screen Interface) (302)~~.

3. (Currently amended) The ~~arrangement~~ apparatus according to claim 1, wherein the memory bus ~~(304)~~ connected to the processor ~~(301)~~ is a non-synchronized memory bus.

4. (Currently amended) The ~~arrangement~~ apparatus according to claim 1, wherein the memory bus ~~(304)~~ is ~~for realizing~~ configured to realize signaling between the processor ~~(301)~~ and a memory unit ~~(303)~~, as well as between the processor ~~(301)~~ and the display device connection interface ~~(302)~~.

5. (Canceled)

6. (Currently amended) The ~~arrangement~~ apparatus according to claim 1, wherein the adapter circuit ~~(402)~~ comprises one or more ~~is provided with~~ gates, ~~(51,54, 57,58, 59,61) in order~~ said gates are configured to match ~~the~~ respective signals ~~(603,604)~~ between the memory bus ~~(401,510)~~ and the display device connection interface ~~(404,540)~~.

7. (Currently amended) The ~~arrangement~~ apparatus according to claim 1, further comprising ~~wherein the arrangement also includes~~ an interference protection ~~segment~~ block connected between the adapter circuit and the display device connection interface, said interference protection block being configured to prevent ~~(403,530) in order to prevent~~ electric interferences among signals.

8. (Currently amended) ~~Method for connecting a display device (303) to a processor (301) controlling the display device~~A method, comprising:

establishing a connection between a memory bus and a display device connection interface, wherein said display device connection interface is integrated in a display device; and

matching signals between the memory bus and the display device,

~~integrating an intelligent connection interface (302) in the display device (303), providing a memory bus (304) for providing signaling between the processor (301) and the display device connection interface (302)~~ wherein the memory bus ~~(304)~~ is connected ~~to the~~ between a processor ~~(301)~~ controlling the display device, and ~~providing~~ an adapter circuit, said adapter circuit is connected between the memory bus and the display device connection interface, and

wherein matching the signals between the memory bus and the display device comprises synchronizing the signals of the memory bus in an order required by the display device by said adapter circuit ~~(402) for adapting signals between the memory bus (401,510) and the display device connection interface (404,540) wherein the signals are adapted to be compatible by said adapter circuit (402)~~.

9. (Currently amended) ~~Method~~ The method according to claim 8, wherein the memory bus ~~(304)~~ connected to the processor ~~(301)~~ is ~~arranged~~ configured to function both as a bus between the processor ~~(301)~~ and a memory unit ~~(303)~~, and a bus between the processor ~~(301)~~ and the display device ~~(303)~~.

10. (Canceled)

11. (Currently amended) The method ~~Method~~ according to claim 8, wherein the memory bus ~~(401)~~ and the display device connection interface ~~(404)~~ are connected by glue logics together in order to achieve communication therebetween.

12. (Currently amended) An adapter circuit, connected between a memory bus and a display device connection interface integrated in a display device, said memory bus having one or more control signal lines and one or more data signal lines for realizing signaling between ~~the~~ a ~~controlling~~ processor ~~(301)~~ and the display device ~~(303)~~, wherein said adapter circuit is configured to match signals between the memory bus and the display device by synchronizing the signals of the memory bus in an order required by the display device~~the signaling between the processor (301) and the display device connection interface (302,404, 540) is realized through said memory bus (304,401, 510) connected to the processor (301), and that the adapter circuit (402) electrically matches the display device connection interface (404,540) and the memory bus (401,510)~~.

13. (Currently amended) ~~Adapter~~ The adapter circuit according to claim 12, wherein the adapter circuit ~~(402)~~ is provided with gates ~~(51,54, 57,58, 59,61)~~ for synchronizing the timing of the signals ~~(603,604)~~ between the display device connection interface ~~(404,540)~~ and the memory bus ~~(401,510)~~, and for combining the display device connection interface ~~(404,540)~~ and the memory bus ~~(401,510)~~ as a physical, uniform bus.

14. (Currently amended) The ~~arrangement~~ method of claim ~~5~~8, wherein the adapter circuit ~~(402)~~ is provided with gates ~~(51, 54, 57, 58, 59, 61)~~ in order to match the signals ~~(603,604)~~ between the memory bus ~~(401,510)~~ and the connection interface ~~(404,540)~~.